WHAT IS CLAIMED IS:

1. A method for reducing metal diffusion in a semiconductor device, comprising:

forming a copper containing metal portion over a substrate;

forming a silicon carbon nitro-oxide (SiCNO) layer on the copper containing metal portion;

depositing a first dielectric layer over the SiCNO layer; and

generating an opening in the SiCNO layer and the first dielectric layer for a connection metal portion to be connected to the copper containing metal portion,

wherein the SiCNO layer reduces the diffusion of the copper containing metal portion into the first dielectric layer.

2. The method of claim 1 wherein the forming a SiCNO layer is performed in a PECVD chamber.

3. The method of claim 1 wherein the forming a SiCNO layer further includes:

depositing a Si based precursor layer; and

exposing the precursor layer to predetermined gases providing C, N, and O elements to form SiCNO.

4. The method of claim 3 wherein the predetermined gases include $SiH(CH_3)_3$ or $Si(CH_3)_4$, CO_2 or O_2, and NH_3.

5. The method of claim 3 wherein the SiCNO is formed under a pressure between 2 and 4 Torr with a temperature between 325 and 400 ^{0}C.

6. The method of claim 1 wherein the SiCNO layer is formed in a HDP deposition chamber.

7. The method of claim 1 wherein the generating further includes:

etching the first dielectric layer and the SiCNO layer to form a trench

region and a via region; and

depositing the connection metal portion into the trench and via regions.

8. The method of claim 7 further includes forming a sealing SiCNO layer on top of the deposited connection metal portion and the first dielectric layer.

9. The method of claim 7 further includes forming a sidewall SiCNO layer on the sidewalls of the via and trench before depositing the connection metal portion.

10. The method of claim 1 further comprising:
reducing the first dielectric layer to a predetermined thickness;
depositing a SiCNO based etch stop layer on top of the reduced first dielectric layer; and
depositing a second dielectric layer on top of the etch stop layer.

11. The method of claim 10 wherein the generating further comprising:
etching the first and second dielectric layers and the SiCNO based etch stop layer to form a trench region and a via region; and
depositing the connection metal portion into the trench and via regions.

12. The method of claim 11 further includes forming a sidewall SiCNO layer on the sidewalls of the via and trench before depositing the connection metal portion.

13. The method of claim 10 further comprising depositing on top of the connection metal portion a sealing SiCNO layer that seals the connection metal portion and the second dielectric layer thereunder.

14. A semiconductor device, comprising:
a copper containing metal layer;
a first silicon carbon nitro-oxide (SiCNO) based diffusion barrier layer covering at least a part of the copper based metal layer for reducing the diffusion of the copper based metal layer;
a dielectric layer on top of the SiCNO layer; and

a conductive material making a metal connection to the copper containing metal layer through an opening in the SiCNO layer and the dielectric layer.

15. The device of claim 14 further comprising a second diffusion barrier layer on top of the conductive material and the dielectric layer.

16. The device of claim 14 further comprising a sidewall diffusion barrier layer coated on the sidewalls of the opening in the SiCNO layer and the dielectric layer.

17. The device of claim 16 wherein the sidewall diffusion barrier layer contains SiCNO.

18. The device of claim 14 further comprising a SiCNO based sealing layer covering the dielectric layer and the conductive material in the opening.

19. A semiconductor device comprising:

a copper containing metal layer;

a first silicon carbon nitro-oxide (SiCNO) based diffusion barrier layer covering at least a part of the copper based metal layer for reducing the diffusion of the copper based metal layer;

a first dielectric layer on top of the SiCNO based diffusion barrier layer;

an etch stop layer covering at least a part of the first dielectric layer;

a second dielectric layer on top of the etch stop layer; and

a conductive material making a metal connection to the copper based metal layer through an opening in the first SiCNO based diffusion barrier layer, the etch stop layer, and the first and second dielectric layers.

20. The device of claim 19 further comprising a second diffusion barrier layer on top of the conductive material and the second dielectric layer.

21. The device of claim 20 wherein the second diffusion barrier layer is SiCNO based.

22. The device of claim 19 further comprising a sidewall diffusion barrier layer coated on the sidewalls of the opening.

23. The device of claim 22 wherein the sidewall diffusion barrier layer is SiCNO based.

24. A method for reducing copper diffusion in a semiconductor device, comprising:

depositing a copper containing metal layer on top of a substrate;

depositing a Si based precursor layer on top of the copper based metal layer;

exposing the precursor layer to predetermined gases to form a silicon carbon nitro-oxide (SiCNO) layer;

depositing a first dielectric layer on top of the SiCNO layer;

reducing the first dielectric layer to a predetermined thickness;

depositing a SiCNO based etch stop layer on top of the reduced first dielectric layer;

depositing a second dielectric layer on top of the etch stop layer;

etching the first and second dielectric layers and the SiCNO based etch stop layer to form a trench region and a via region;

depositing a predetermined metal into the trench and via regions to contact the copper based metal layer;

wherein the SiCNO layer prevents the diffusion of the copper based metal layer into the first dielectric layer.

25. The method of claim 24 further comprising depositing on top of the trench a sealing SiCNO layer that seals the trench and second dielectric layer thereunder.

26. The method of claim 24 further comprising forming a sidewall SiCNO layer covering the sidewals of the trench and via regions.